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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,667	12/28/2001	Seung-Kyu Choi	3430-0172P	3666

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EXAMINER	
LANDAU, MATTHEW C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,667	CHOI ET AL.	
	Examiner	Art Unit	
	Matthew Landau	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5-9,11,12,14 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2 and 5* is/are allowed.

6)☒ Claim(s) *6-9 and 11* is/are rejected.

7)☒ Claim(s) *14 and 22* is/are objected to.

8)☐ Claim(s) ___ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Han in view of Lyu.

In regards to claims 6 and 8, Figures 4 and 6B of Han disclose a substrate 110; gate and data lines (117 and 115) crossing each other on the substrate; a thin film transistor having a gate electrode 107 extending from the gate line, a semiconductor layer 111, first and second ohmic contact layers 112, and source and drain electrodes (105 and 106), a passivation layer 113a pattern on the data line and the thin film transistor, the passivation layer pattern exposing a portion of a side surface of the drain electrode; and a pixel electrode 104 connected to the drain electrode; and a gate insulation film 109 formed directly on the gate insulation film at a pixel region defined by the gate and data lines. It is considered that the slanted portion of the drain electrode 106 is "a side surface", since it is a side of the upper portion of the drain electrode. The difference between Han and the claimed invention is the semiconductor layer and the ohmic contact layers having ends aligned with and directly below corresponding ends of the source electrode and drain electrodes. Figure 3I of Lyu discloses a thin film transistor with a semiconductor layer 137 and ohmic contact layers 139 having ends aligned with and directly below the corresponding ends of the source and drain electrodes. In view of such teaching, it

would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Han by using the layer alignment of Lyu for the purpose of simplifying the production process and reducing manufacturing costs.

In regards to claim 7, Figures 4 and 6B of Han disclose a storage capacitor including a first storage electrode 117, a portion of a gate insulation layer 109, and a second storage electrode 130, and wherein the pixel electrode 104 contacts the second storage electrode through a contact hole formed through the passivation layer.

In regards to claim 9, Figure 6B of Han discloses the passivation layer pattern exposes a portion of only one side surface of the drain electrode.

In regards to claim 11, Figure 6B of Han discloses the passivation layer 113a pattern further exposes a portion of a top surface of the drain electrode.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kwak et al. (US Pat. 6,509,940, hereinafter Kwak) in view of Lyu.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the

application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). This rejection might also be overcome by showing that the reference is disqualified under 35 U.S.C. 103(c) as prior art in a rejection under 35 U.S.C. 103(a). See MPEP § 706.02(l)(1) and § 706.02(l)(2).

In regards to claim 12, Figures 3 and 4 of Kwak disclose an array substrate for a liquid crystal display device, comprising: a substrate 31; a gate line 34 on the substrate; a gate insulator 35 on the gate line; a semiconductor layer 37 on the gate insulator; a first ohmic contact layer 39 (left side) and a second ohmic contact layer 39 (right side) on the semiconductor layer; a data line 24 and source and drain electrodes (41 and 43) on the plurality of ohmic contact layers, the source electrode connected to the data line, the drain electrode facing and spaced apart from the source electrode; a passivation layer 45 on the source and drain electrodes and covering a crossing portion of the gate and data lines, a portion of a side surface of the drain electrodes being exposed; a pixel electrode 49 connected to the drain electrodes; wherein the gate insulator comprises a gate insulation film 35 formed over the gate line, wherein a portion of the pixel electrode is formed directly on the gate insulation film at a pixel region defined by the gate and data lines, wherein the pixel electrode contacts side portions of the semiconductor layer and the second ohmic layer, wherein the second ohmic contact layer has an end aligned with and directly below an end of the drain electrode. The difference between Kwak and the claimed invention is the semiconductor layer and the first ohmic contact layer having ends aligned with and directly below the end of the source electrode. Figure 3I of Lyu discloses a thin film transistor with a semiconductor layer 137 and ohmic contact layers 139 having ends aligned with and directly

below the corresponding ends of the source and drain electrodes. In view of such teaching, it would have been obvious to the ordinary artisan at the time the invention was made to modify the invention of Kwak by using the layer alignment of Lyu for the purpose of simplifying the production process and reducing manufacturing costs (see abstract of Lyu).

Allowable Subject Matter

Claims 1, 2, and 5 are allowed.

Claims 14 and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for allowance:

Regarding claim 1, the prior art of record, either singularly or in combination, does not disclose or suggest the combination of limitations including a storage capacitor including a portion of the gate line as a first storage electrode, a portion of the gate insulation layer, and a second storage electrode having an island shape, wherein the second storage electrode is disposed directly contacting the gate insulation layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

Applicant's arguments filed July 13, 2004 have been fully considered but they are not persuasive.

In response to Applicant's arguments regarding claim 6 that the motivation to combine Han and Lyu "is not supported by objective evidence of record and is improperly based solely on speculation unsupported by objective evidence of record", it is respectfully noted that the motivation cited by the examiner finds support in the abstract of Lyu. In the abstract, Lyu states that the semiconductor layers are patterned and etched at the same time as the source and drain metallizations, and that using this single etch process reduces manufacturing costs. As shown in Figure 3F of Lyu, patterning and etching the source/drain electrodes at the same time as the semiconductor layers results in the ends being aligned (as claimed). Applicant further argues that Han discloses "the contact hole exposing a top surface of the drain electrode 106, not the side surface". This is not found persuasive since the slanted portion at approximately the middle of the drain electrode 106 can be considered a side surface, since it is facing to the right. Furthermore, the top surface itself can be considered a side surface, since it could be referred to as the "top side". For instance, a cube has six sides and one of those sides could be called the top side.

Applicant's arguments regarding claim 12 are moot in light of the new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Landau whose telephone number is (571) 272-1731.

The examiner can normally be reached from 8:30 AM - 5:30 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER

Matthew C. Landau

Examiner

April 27, 2005